Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination – June – 2017**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Code :** | **14EC3024** | **Duration :** | **3hrs** |
| **Sub. Name :** | **LOW POWER VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | A 32 bit off-chip bus operating at 3V and 700 MHz clock rate is driving a capacitance of 35pF/ bit. Eachbit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation inoperating the bus? | CO3 | 5 |
| b. | Derive an expression for dynamic power dissipation in a CMOS inverter due to charging and discharging ofcapacitance. | CO1 | 9 |
| c. | Explain about architectural level power analysis. | CO1 | 6 |
| (OR) | | | | |
| 2. | a. | The chip size of a CPU is 20mm x 45 mm with clock frequency of 800MHz operating at 2.5 V. The length ofthe clock rouing is estimated to be twice the circumference of the chip. Assume that the clock frequency isrouted on a metal layer with width of 1.2µm and the parasitic capacitance of the metal layer is 2.5 Ff/µm2. What isthe power dissipation of the clock signal? | CO3 | 5 |
| b. | Discuss the variation of short circuit current of a CMOS inverter for input signal slope and output loadcapacitance. | CO1 | 10 |
|  | c. | Derive an expression which relates static probability and frequency. | CO3 | 5 |
| 3 | a. | Explain in detail about the power and delay of an inverter chain using transistor sizing. | CO1 | 8 |
|  | b. | Explain in detail about Equivalent Pin Ordering and Network Restructuring and Reorganization. | CO1 | 12 |
| (OR) | | | | |
| 4 | a. | Discuss state machine encoding with an example. | CO1 | 6 |
|  | b. | Explain the architecture of Bus invert encoding. Analyze its performance in terms of efficiency. | CO1 | 14 |
| 5. | a. | Discuss in detail about the Precomputation Logic Technique with an example. | CO1 | 14 |
|  | b. | How to take precautions to avoid floating node in CMOS circuits to reduce power consumption. | CO1 | 6 |
| (OR) | | | | |
| 6. | a. | Explain in detail various Power Reduction Techniques in Clock Networks. | CO3 | 14 |
|  | b. | Explain in detail the power management techniques to reduce power in architecture level. | CO3 | 6 |
| 7. | a. | Show how parallelism has been used to improve  computationthroughput of high performance digitalsystems. | CO3 | 10 |
|  | b. | Explain in detail the organization of a RAM and also explain the operation of 6T MOS static RAM memory cell. | CO2 | 10 |
| (OR) | | | | |
| 8. | a. | Explain the deep sub micrometer device design issues and the key  tominimize short channel effects. | CO3 | 6 |
|  | b. | Explain in detail the Low Voltage circuit design techniques | CO3 | 14 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Explain the concepts of energy recovery circuit design. | CO1 | 10 |
|  | b. | Explain the methods of reducing power in Writer Driver circuits and Sense Amplifier circuits of SRAM core. | CO2 | 10 |

ALL THE BEST

**Course Outcome:**

CO1: Students will get knowledge in low power techniques.

CO2: To design low power SRAMs.

CO3: To design chips with low power consumption and high performance circuits.